

FIG. 1

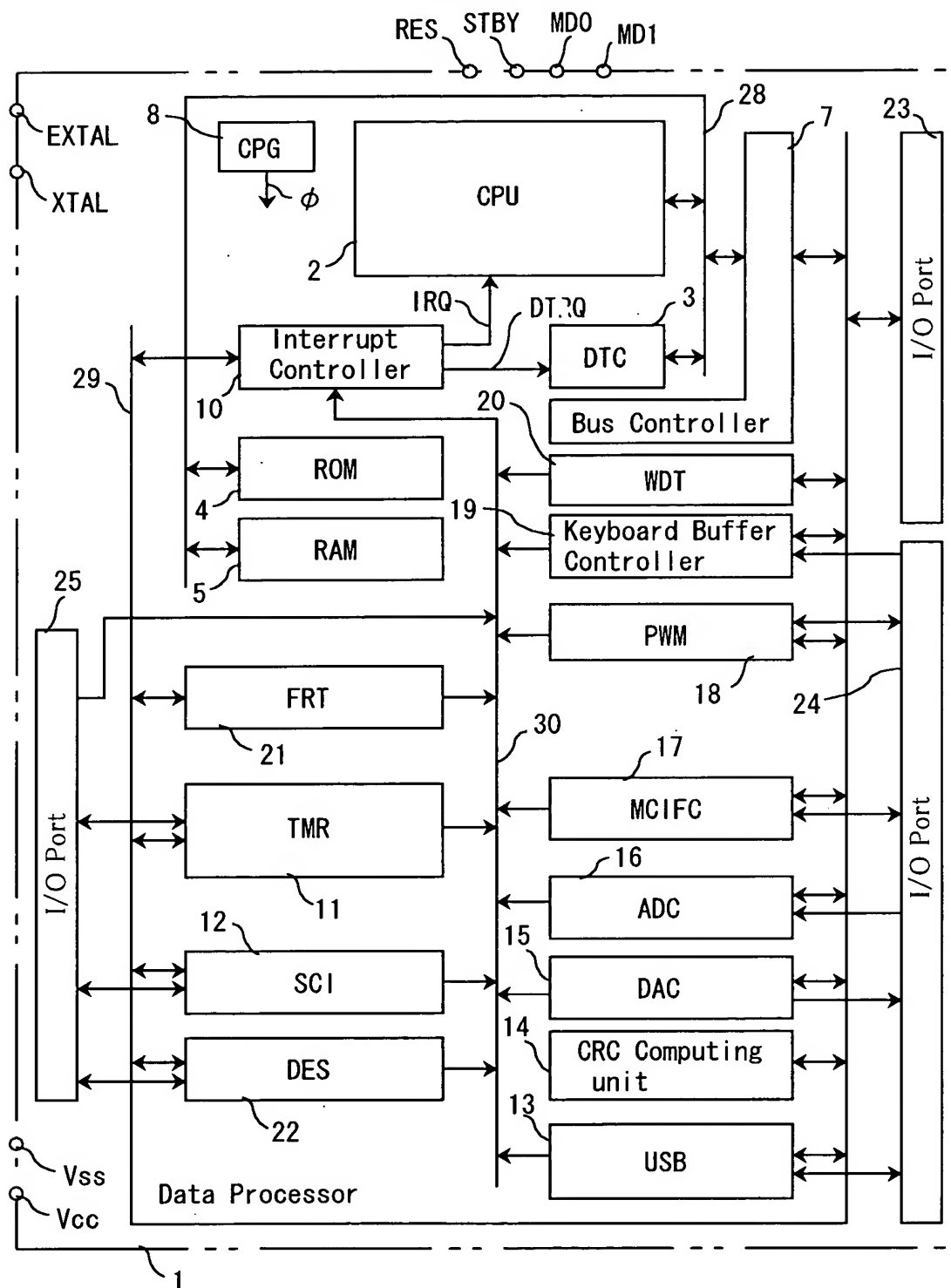
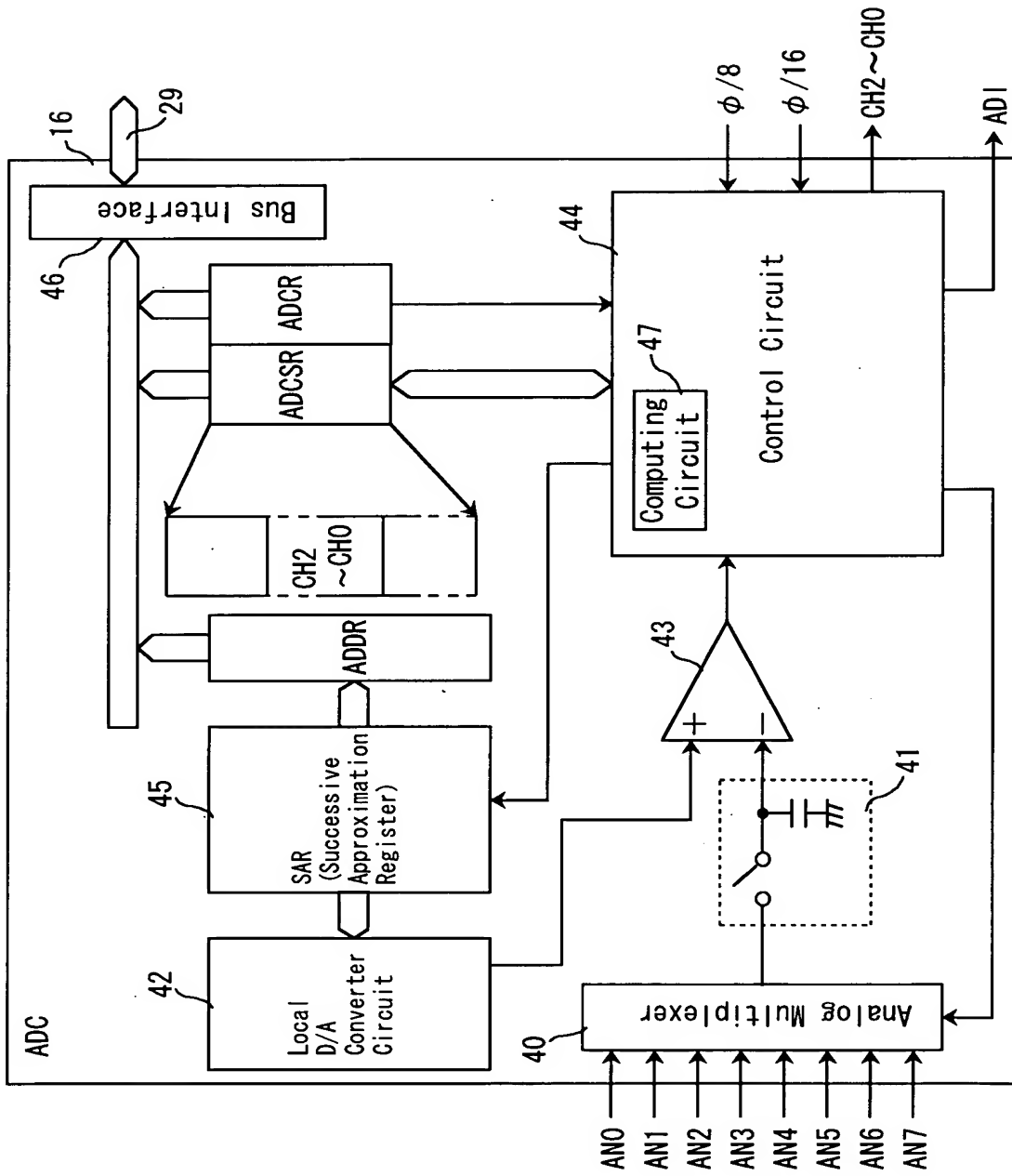


FIG. 2



3. 6. 11

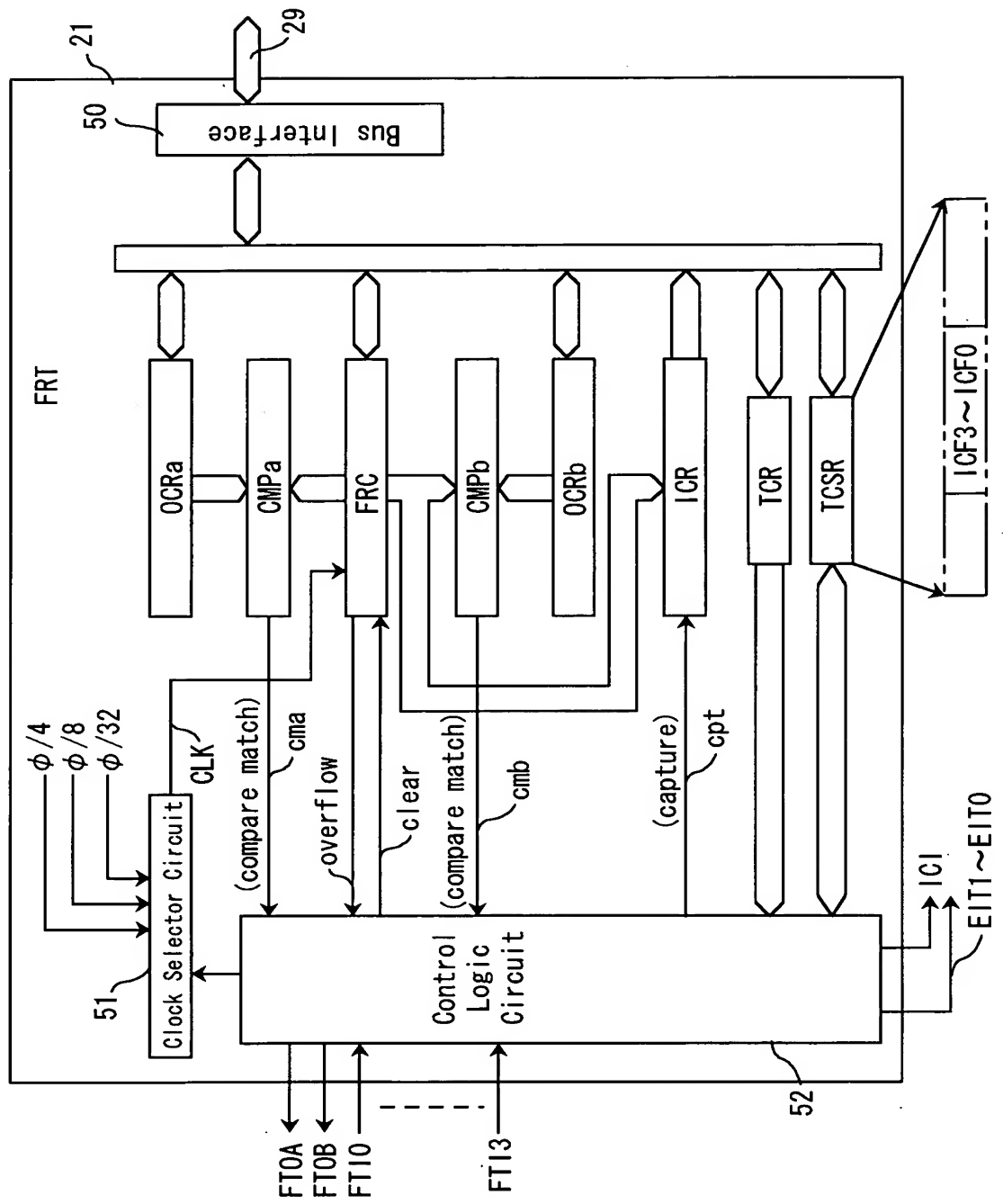


FIG. 4

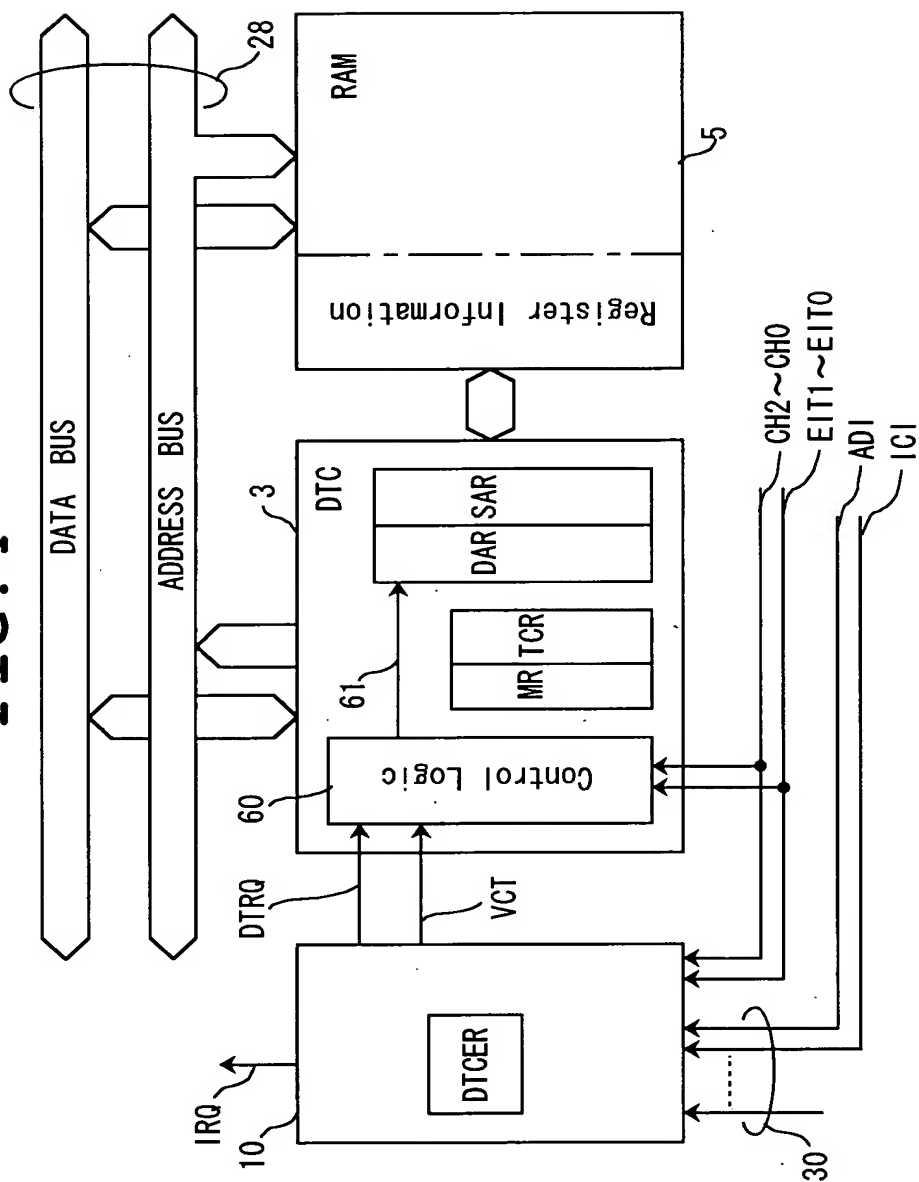


FIG. 5

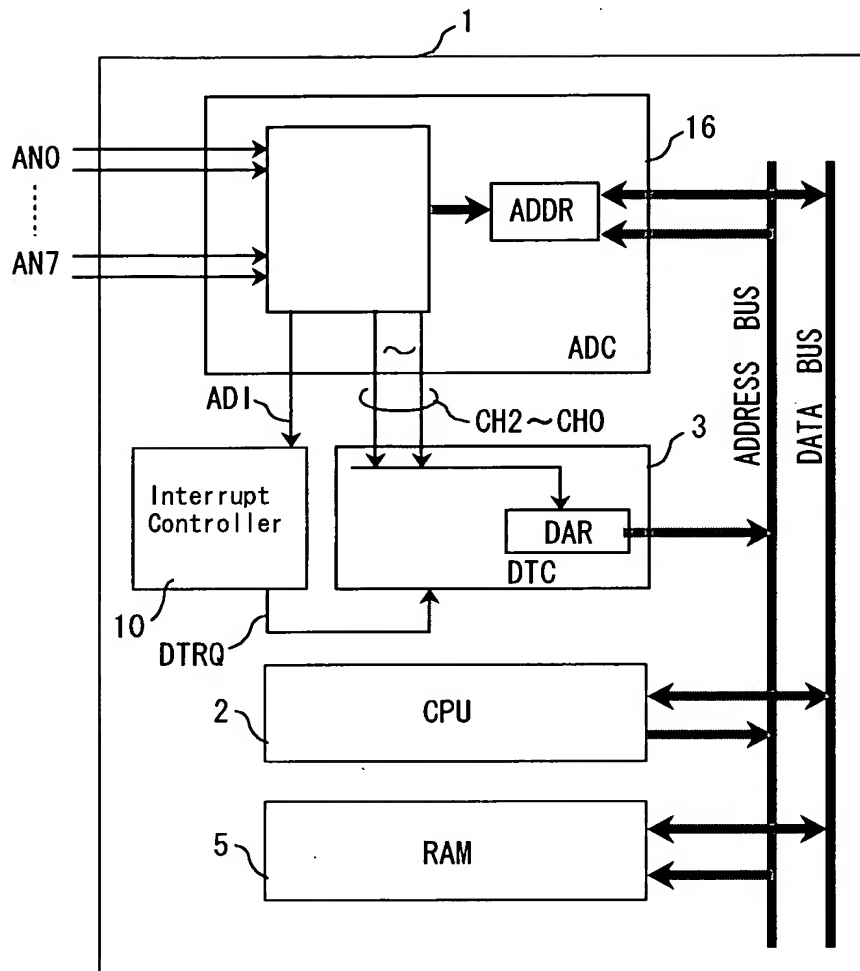


FIG. 6

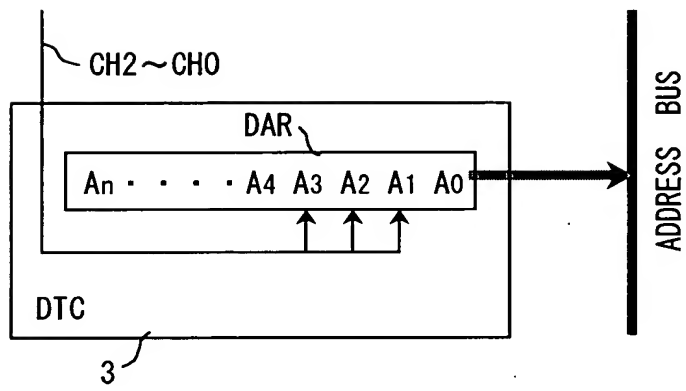


FIG. 7

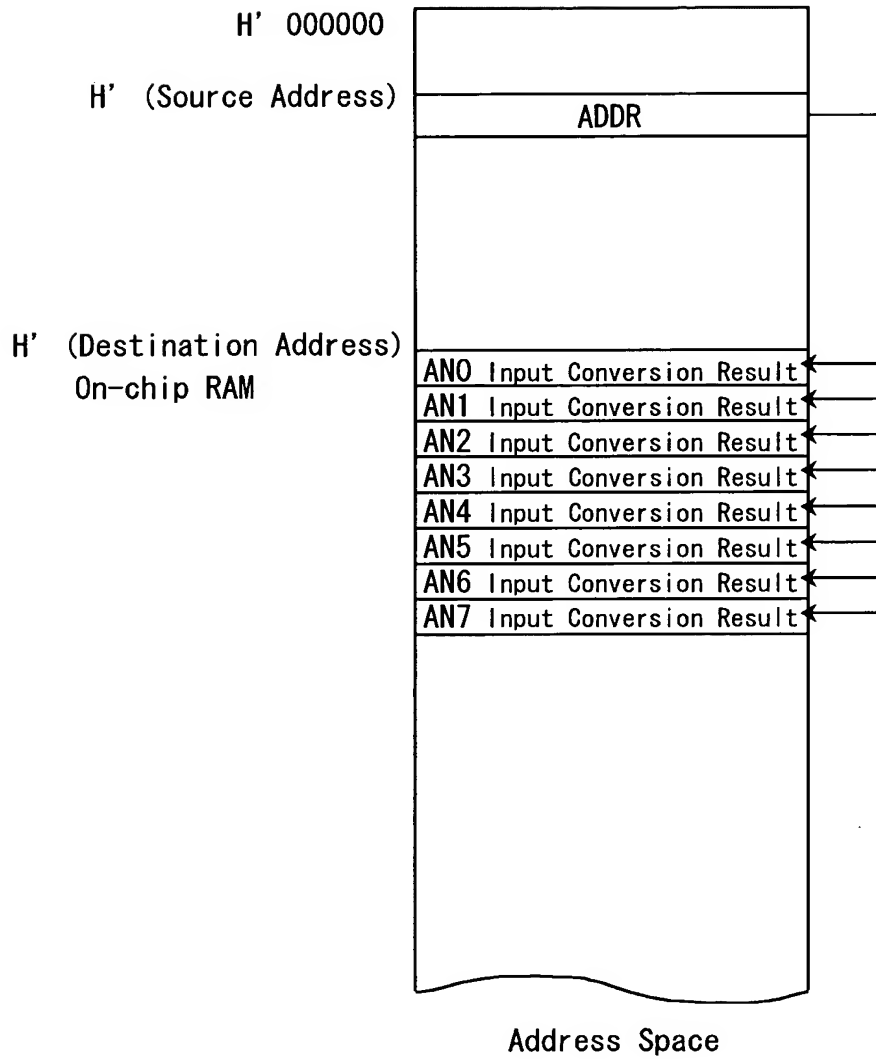


FIG. 8

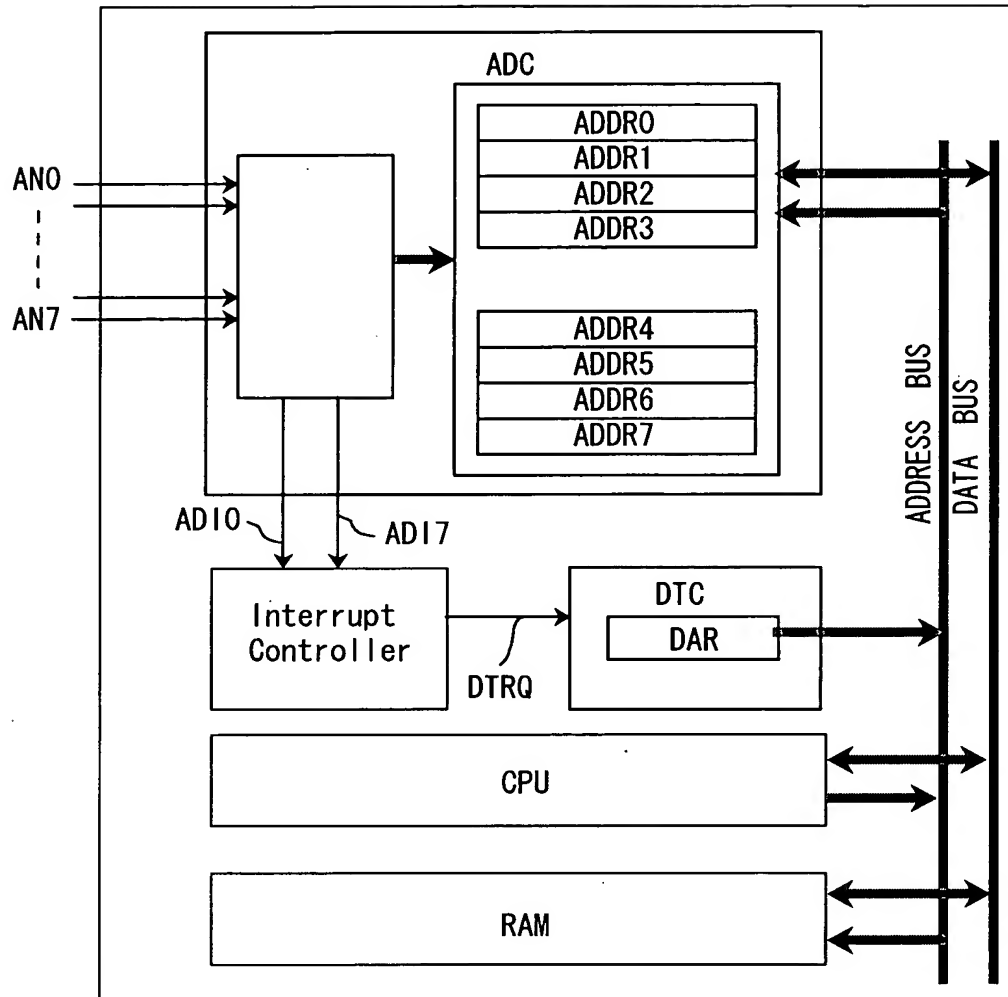


FIG. 9

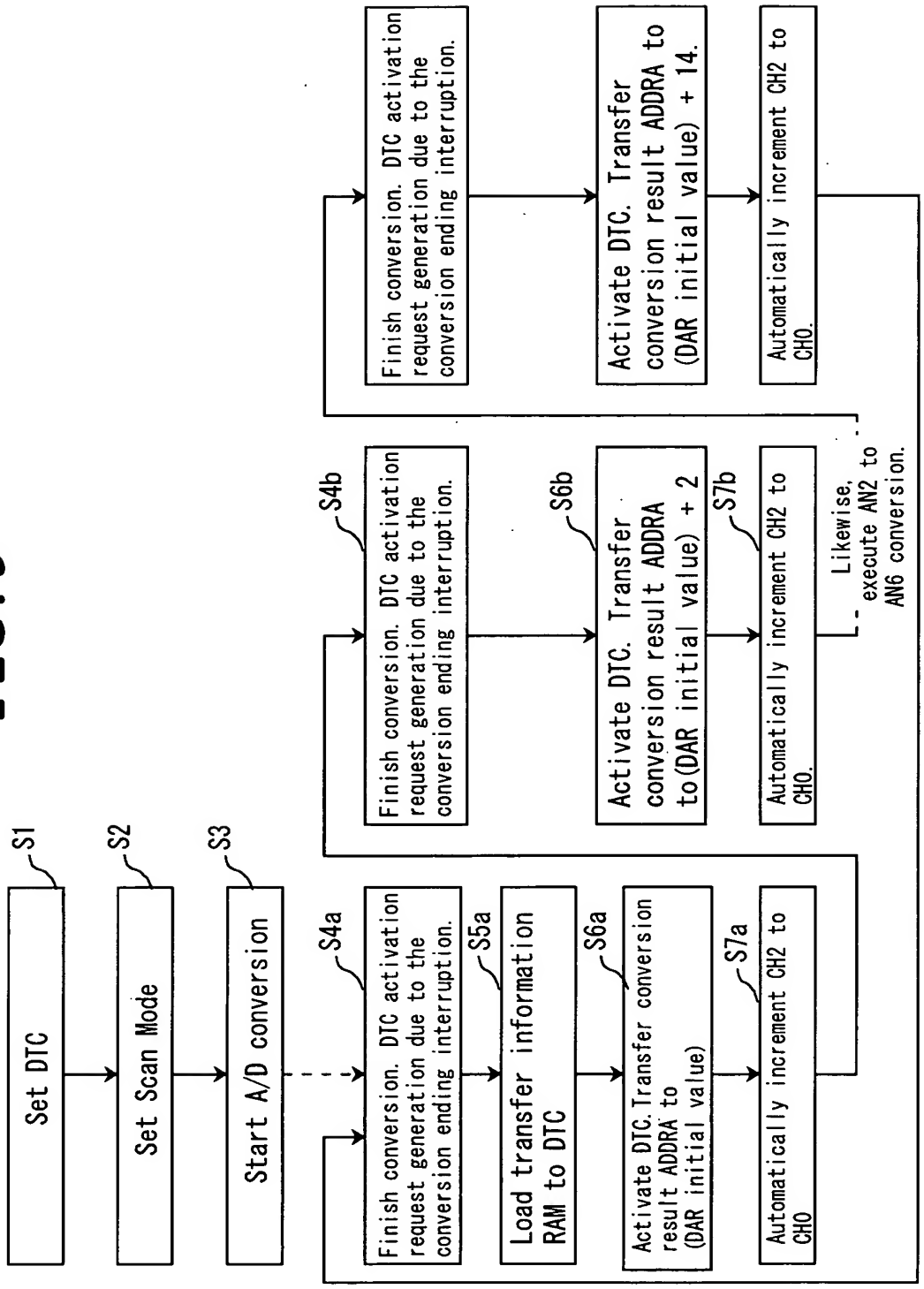


FIG. 10

CH2	CH1	CH0	DAR				A/D conversion
			A3	A2	A1	A0	
0	0	0	0	0	0	0	AN0 Input Conversion
0	0	1	0	0	1	0	AN1 Input Conversion
0	1	0	0	1	0	0	AN2 Input Conversion
0	1	1	0	1	1	0	AN3 Input Conversion
1	0	0	1	0	0	0	AN4 Input Conversion
1	0	1	1	0	1	0	AN5 Input Conversion
1	1	0	1	1	0	0	AN6 Input Conversion
1	1	1	1	1	1	0	AN7 Input Conversion

FIG. 11

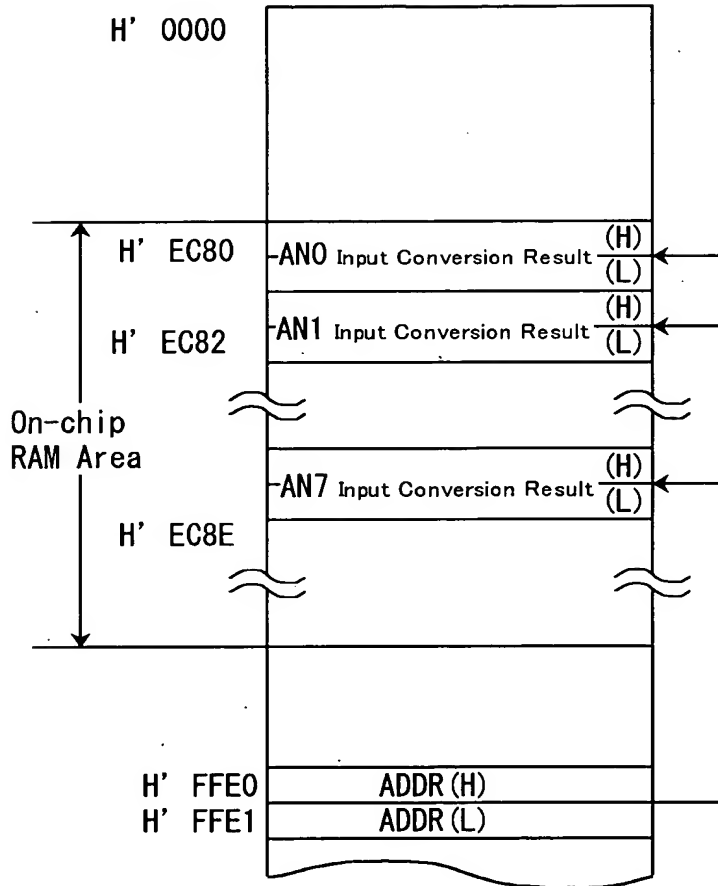


FIG. 12

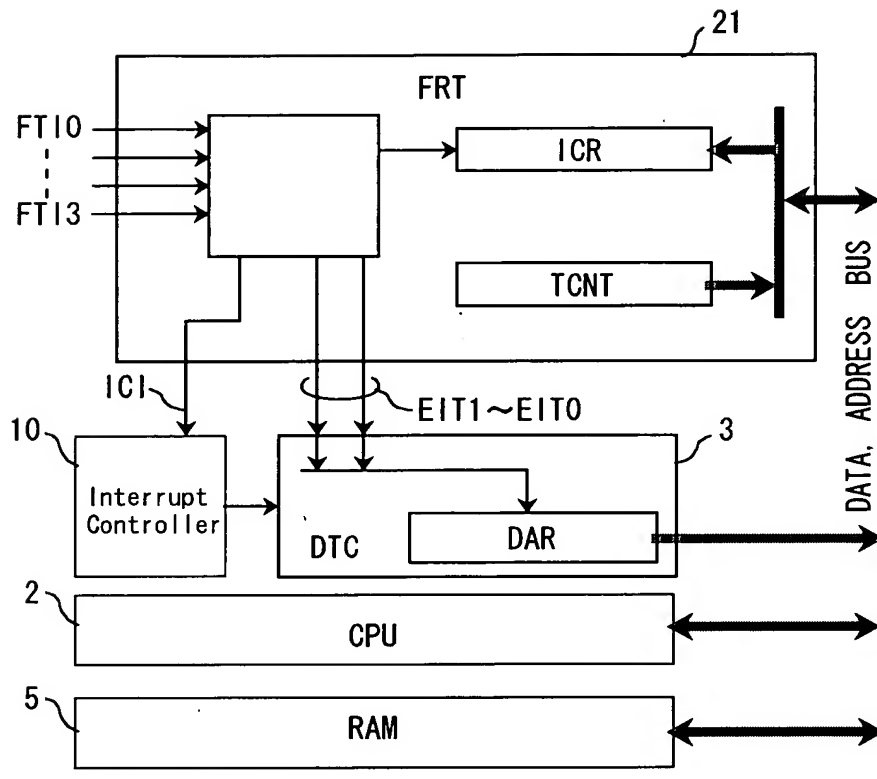


FIG. 13

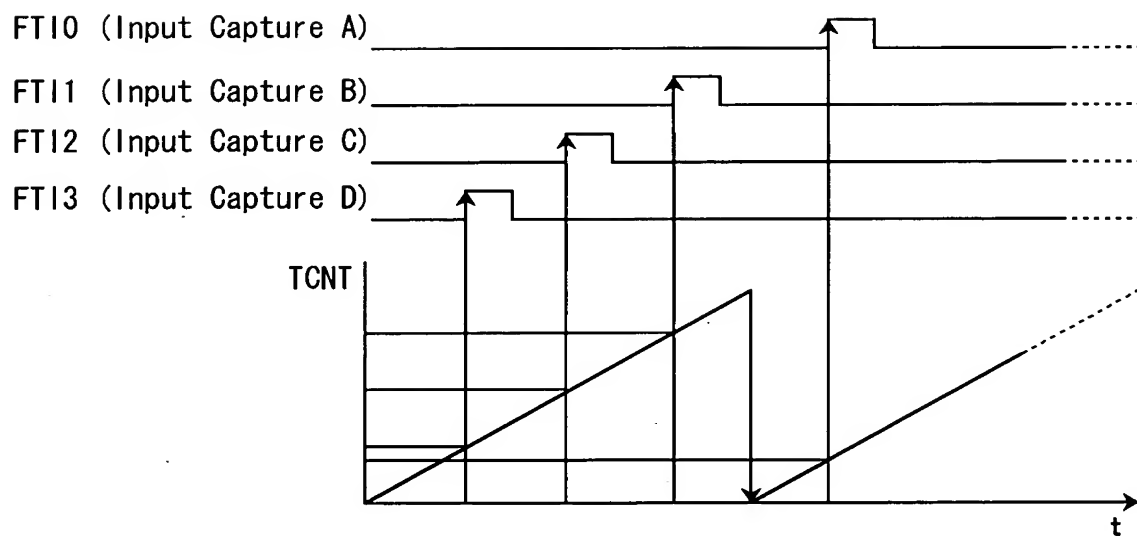


FIG. 14

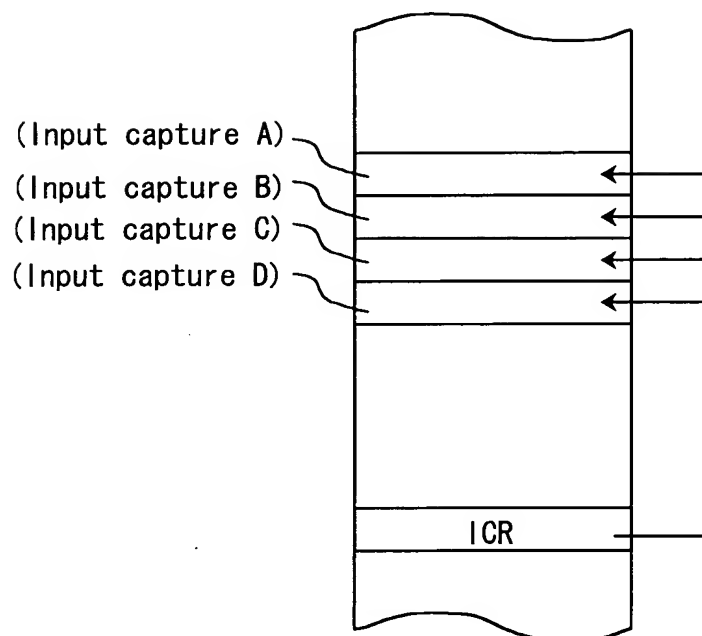


FIG. 15

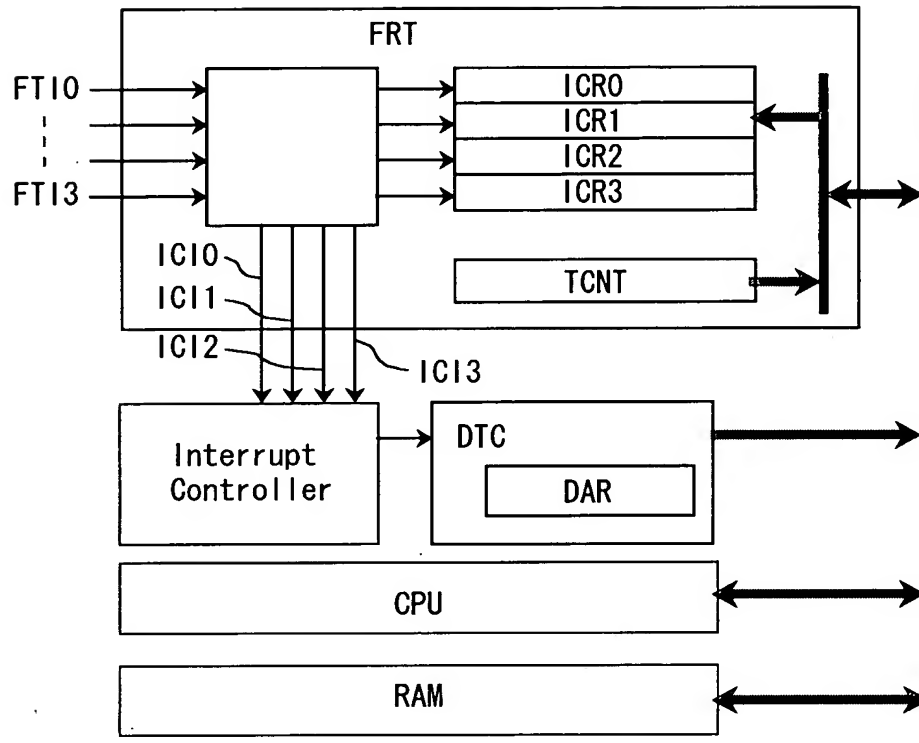


FIG. 16

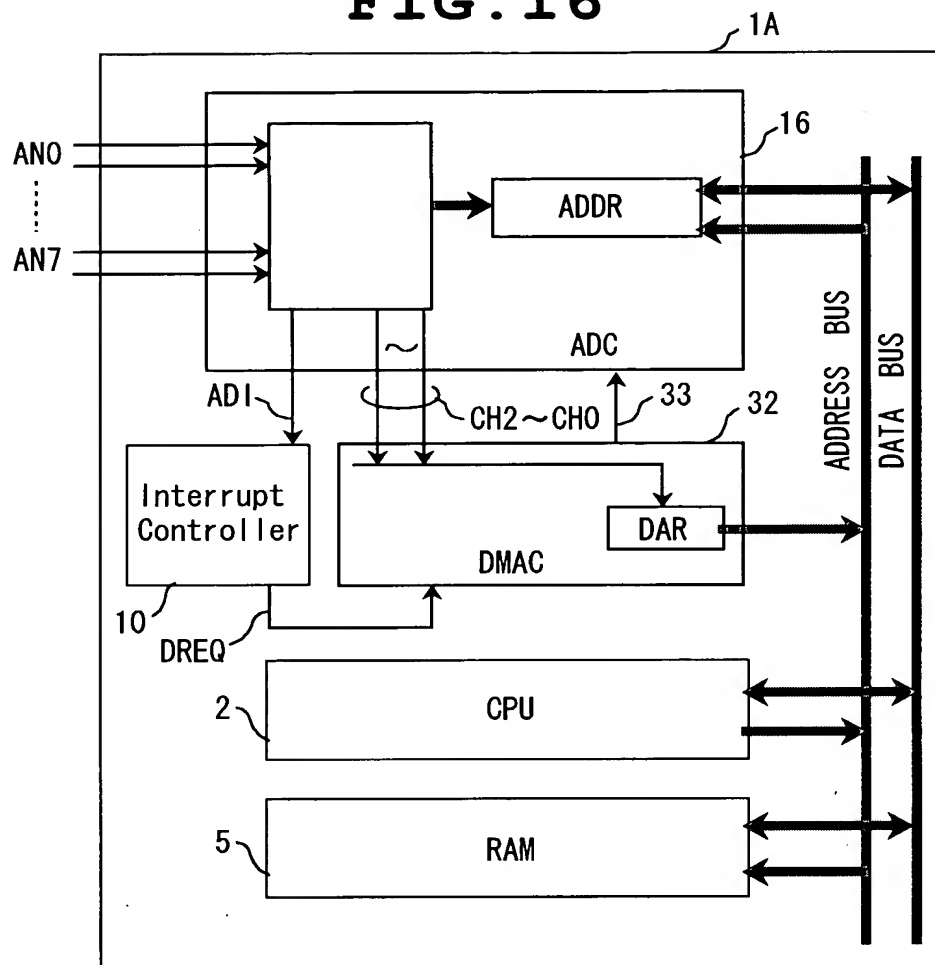


FIG. 18

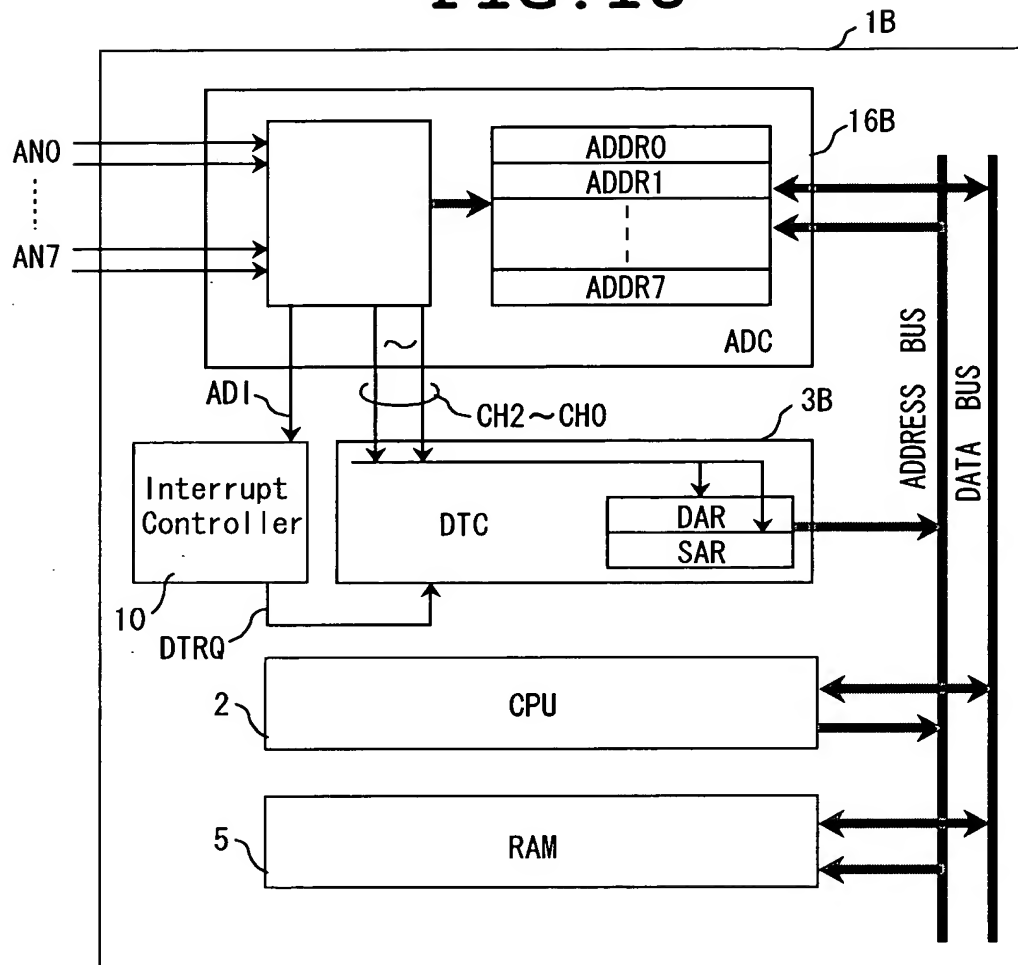


FIG. 19

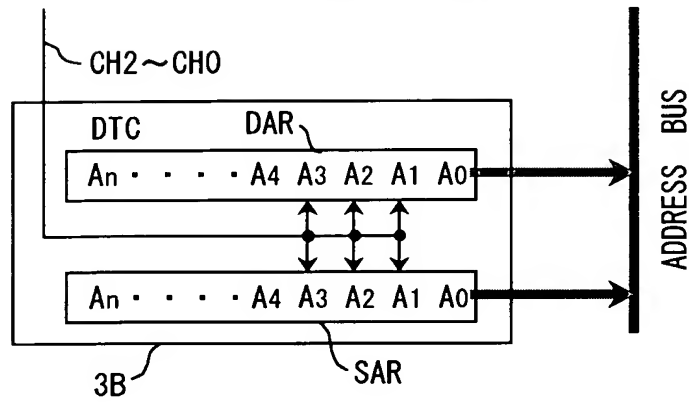


FIG. 20

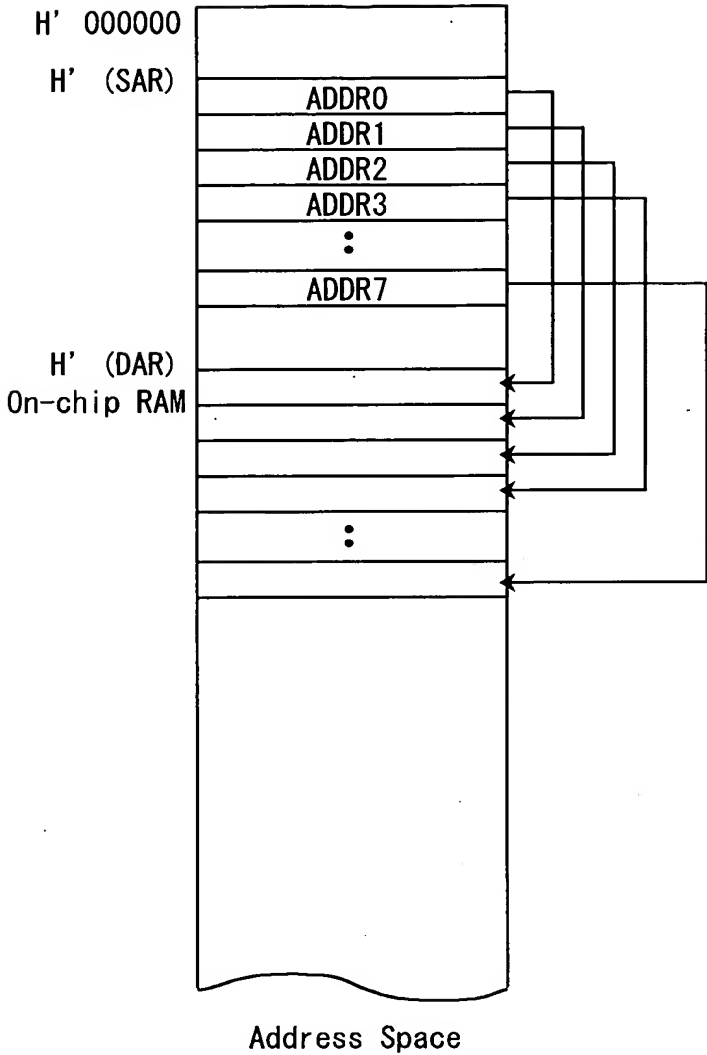


FIG. 21

